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10/606,419	06/26/2003	Vigyan Singhal	TFI-003	4881

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EXAMINER	
TO, TUYEN P	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 07/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/606,419	SINGHAL ET AL.	
	Examiner	Art Unit	
	Tuyen To	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7,15, and 30* is/are rejected.

7)☒ Claim(s) *6,8-14,16-29 and 31-40* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 June 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a response to the communication filed on 06/26/2003. Claims 1- 40 are pending.

Claim Objections

1. **Claims 5 –12** are objected because the recited " the articulated fan-in " lacks of antecedent basis.

Claim 1 is objected because the recited " modifying the analysis" in step (c) lacks of antecedent basis.

Claim 37 is objected because the recited " the verified user defined rules" in step (c) and " the articulation points" in step (e) lack of antecedent basis.

Claim 1, 27, and 29 are objected because the " in (a) false" recited in claims 1(step c), 27, and 29 (step d) is not clear and should be reworded.

Claims 38-40 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

Claim 6 is objected because the phrase " the group of primary inputs, storage elements and articulation points" is not in the proper Markush-type claim format. Examiner suggests rephrasing as " the group consisting of primary inputs, storage elements and articulation points".

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

3. The listings of references in the specification (in pages 3 and 9) are not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609 A(1) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered.

Drawings

4. The drawings are objected to because Figures 1-16 do not comply with 37 CFR 1.84(m). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> *(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.*

6. **Claims 1-5, 7, 15, and 30** are rejected under 35 U.S.C. 102(e) as being anticipated by Singhal et al. (Singhal) (US Pub. No. 2003/0208730).

The applied reference has a common assignee (Tempus Fugit Inc.) with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Referring to claim 1, Singhal discloses the method for guiding formal verification for a circuit design in circuit simulation software to optimize the time required for verification of the circuit design, the method comprising the steps of:

a. identifying an analysis region for verifying the circuit design (*p. 10, claim 1, step d*);

b. verifying the circuit design by applying formal verification over the analysis region (*p. 10, claim 2, step d*);

c. manually modifying the analysis if verification of the circuit design over the analysis region results in false (*p.10, claim 2, step f; page 11, claim 10*);

repeating steps b-c until the circuit design is verified (*p. 10, claim 2; page 11, claim 10*); and

repeating steps b-c until a user identifies an error in the circuit design (*p. 10, claim 2; page 11, claim 10*).

Referring to claim 2, Singhal discloses the method according to claim 1, wherein the step of manually modifying the analysis comprises the steps of:

a. selecting a signal in the analysis region (*p.11, claim10, step a*) and

b. adding a portion of the circuit design relating to the signal in the analysis region (*p.11, claim10, step b).*

Referring to claim 3, Singhal discloses the method according to claim 2, wherein the step of selecting the signal in the analysis region is performed by selecting the signal from a Plot window (p.11, *claim10, step a*; page *1 [0004]*).

Referring to claim 4, Singhal discloses the method according to claim 2, wherein the step of selecting the signal in the analysis region is performed by selecting the signal from a Source Code window *(p.11, claim10, step a; page 1 [0004]*).

Referring to claim 5, Singhal discloses the method according to claim 2, wherein the step of adding a portion of the circuit design relating to the signal in the analysis region

comprises adding the articulated fan-in driving the signal to the analysis region (*page 9[0124]; page 11, claim 10(step b)).*

Referring to claim 7, Singhal discloses the method according to claim 2, wherein the step of adding a portion of the circuit design relating to the signal in the analysis region comprises adding a portion of the articulated fan-in driving the signal to the analysis region (*page 9[0124]; page 11, claim 13, step b).*

Referring to claim 15, Singhal discloses the method for guiding formal verification for a circuit design in circuit simulation software td optimize time required for verification process, the method comprising the steps of:

a. identifying an analysis region for verifying the circuit design (*p. 10, claim 1, step d*);

b. verifying the circuit design by applying formal verification over the analysis region (*p. 10, claim 2, step d);*

c. identifying candidate signals for modification of the analysis region if verification of the circuit design is false(Fig.12 ; page 6 [0085]).

d. automatically modifying the analysis region using the candidate signals(*Fig.12; page 6[0085]),* and

e. manually modifying the analysis region if there are no appropriate candidate signals *(Fig.12; page 6 [0085]; page 2 [0023]);*

repeating steps b-e until the circuit design is verified (*Fig.12; page 7 [0096]),* and

repeating steps b-e until a user identifies an error in the circuit design *(Fig.12; 7 [0096]).*

Referring to claim 30, Singhal discloses the system for guiding formal verification of a circuit design in circuit simulation software to optimize time required for verification process, the system comprising:

a. a GUI for enabling a user to input information (*page 1 [0004]; page 2 [023]; page 12, claim 27; a GUI is inherently a part of a computer system for circuit simulation in circuit design);*

b. an Analysis region Selection tool for selecting an analysis region for verifying the circuit design (*page 2 [0013]*);

c. a Formal verification tool for verifying the circuit design using the selected analysis region and the verified user defined rules (*page 1 [0004] and [0009]);*

Allowable Subject Matter

7. **Claims 6, 8-14, 16-28, and 31-36** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. **Claim 29 and 37** contain allowable subject matter.

9. *The following is a statement of reasons for the indication of allowable subject matter:*

Claim 6 would be allowable because the prior art does not teach or suggest the method for guiding formal verification, wherein the step of manually adding the articulated fan-in driving the signal to the analysis region comprises identifying the articulated fan-in of the signal by traversing the circuit design backwards from the signal until a signal from the group of primary inputs, storage elements and articulation points is encountered.

Claim 8 would be allowable because the prior art does not teach or suggest the method for guiding formal verification, wherein the step of manually adding a portion of the articulated fan-in driving the signal to the analysis region comprises adding a portion of the articulated fan-in driving the selected signal that is "turn-on" by current value assignments in the Plot window to the analysis region.

Claim 9 would be allowable because the prior art does not teach or suggest the method for guiding formal verification, wherein the step of manually modifying the analysis comprises the steps of:

a. selecting a signal in the Plot window at time cycle just after the circuit design is reset ; and

b. adding the reset portion of the articulated fan-in of the selected signal in the analysis region.

Claim 10 would be allowable because the prior art does not teach or suggest the method for guiding formal verification, wherein the step of manually modifying the analysis comprises the steps of:

a. selecting a signal in a Plot window at a time cycle other than just after the circuit design is reset; and

b. adding a non-reset portion of the articulated fan-in of the selected signal in the analysis region.

Claim 11 would be allowable because the prior art does not teach or suggest the method for guiding formal verification, wherein the step of manually modifying the analysis comprises the step of:

a. the user selecting an articulation point inside the analysis region; and

b. removing the articulated fan-in of the articulation point from the analysis region;

Claim 12 would be allowable because the prior art does not teach or suggest the method for guiding formal verification, wherein the step of manually modifying the analysis comprises the steps of:

a. the user selecting an articulation point at the boundary of the analysis region; and

b. adding the articulation fan-in driving the selected articulation point to the analysis region.

Claim 13 would be allowable because the prior art does not teach or suggest the method for guiding formal verification, wherein manually modifying the analysis comprises the steps of:

a. the user selecting at least one signal in the analysis region from the Plot window, wherein each signal is selected at a specific time cycle;

b. generating a triple based on each selected signal, wherein a triple comprises the name of the selected signal, the specific time cycle of selection and the value of the selected signal at the specific time cycle;

c. generating a rule based on the triples;

d. verifying the rule separately; and

e. verifying the circuit design using the rule as an assumption for the analysis region.

Claim 14 would be allowable because the prior art does not teach or suggest the method for guiding formal verification, wherein the rule is automatically modified in case the step of verifying of the rule results in non-verification.

Claim 16 would be allowable because the prior art does not teach or suggest the method for guiding formal verification, wherein the step of identifying the candidate signal for modification of the analysis region if verification of the circuit design is false comprises identifying articulation points corresponding to the analysis region as the candidate signals.

Claim 17 would be allowable because the prior art does not teach or suggest the method for guiding formal verification, wherein the step of automatically identifying articulation point corresponding to the analysis region comprises the steps of:

a. identifying comparison statements on wide signals as articulation points; and

b. identifying Boolean guards of conditional statements as articulation points.

Claim 18 would be allowable because the prior art does not teach or suggest the method for guiding formal verification, wherein the step of automatically modifying the analysis region using the candidate signals include prioritizing the candidate signals on the basis of productivity choices.

Claim 19 would be allowable because the prior art does not teach or suggest the method for guiding formal verification, wherein the step of prioritizing candidate signals on the basis of productivity choices comprises the steps of:

a. assigning productivity weights to analysis region modification choices;

b. ranking the choices according to the productivity weights wherein the choices with positive productivity weights are considered as high- productivity choices and the choice with negative weights are considered low-productivity choices; and

c. identifying the highest-productivity choices from the high-productivity choices.

Claim 20 would be allowable because the prior art does not teach or suggest the method for guiding formal verification, wherein the step of automatically modifying the analysis region comprises expanding the analysis region by including the articulated fan-in corresponding to the highest -productivity choices that are located at the boundary of the analysis region.

Claim 21 would be allowable because the prior art does not teach or suggest the method for guiding formal verification, wherein the step of automatically modifying the analysis region comprises removing the articulated fan-in corresponding to the highest -productivity choices that are located inside the analysis region from the analysis region.

Claim 22 would be allowable because the prior art does not teach or suggest the method for guiding formal verification, wherein the step of automatically modifying the analysis region comprises modifying the analysis region using low-productivity choices on the user's decision in case there are no high-productivity choices.

Claim 23 would be allowable because the prior art does not teach or suggest the method for guiding formal verification, wherein the step manually modifying analysis if there are no appropriate candidate signals, comprises the steps of:

a. defining an abstraction created in response to the low productivity choices in the analysis region; .

b. proving the abstraction in the circuit design separately; and

c. verifying the circuit design using the abstraction in the analysis region.

Claim 24 would be allowable because the prior art does not teach or suggest the method for guiding formal verification, wherein the step of defining an abstraction comprises adding new logic to the circuit design corresponding to the abstraction.

Claim 25 would be allowable because the prior art does not teach or suggest the method for guiding formal verification, wherein the step of manually modifying the analysis if there are no appropriate candidate signals, comprises the steps of:

a. defining an assumption created in response to low productivity choices in the analysis region;

b. proving the assumption in the circuit design separately; and

c. verifying the circuit design using the assumption in the analysis region.

Claim 26 would be allowable because the prior art does not teach or suggest the method for guiding formal verification, wherein the step of manually modifying the analysis includes the steps of:

a. the user selecting at least one signal in the analysis region from a Plot window, wherein each signal is selected at a specific time cycle;

b. generating a triple base on each selected signals, wherein a triple comprises the name of the selected signal, specific time cycle of selection and the value of the selected signal at the specific time cycle;

c .generating a rule based on the triples;

d. verifying the rule separately, and

e. verifying the circuit design using the rule as an assumption for the analysis region.

Claim 27 would be allowable because the prior art does not teach or suggest the method for guiding formal verification, wherein the rule is automatically modified in case the step of verifying of the rule results in a false.

Claim 28 would be allowable because the prior art does not teach or suggest the method for guiding formal verification, wherein the step of manually verifying the circuit design by applying formal verification over the analysis region comprises user deciding that there is an error in the circuit design in case there are no high-productivity choices.

Claim 29 would be allowable because the prior art does not teach or suggest the method for guiding formal verification, for a circuit design in circuit simulation software to optimize the time required for the verification process, the method comprising the steps of:

a. identifying an analysis region for verifying the circuit design

b. verifying the circuit design by applying formal verification over the analysis region;

c. identifying articulation points corresponding to the analysis region as analysis region modification choices;

d. automatically modifying the analysis region using the articulated fan-in of the analysis region modification choices if verification of the digital design over the analysis region results in a false;

repeating steps b-d until the circuit design is verified; and

repeating steps b-d until a user identifies an error in the circuit design.

Claim 31 would be allowable because the prior art does not teach or suggest the system for guiding formal verification, wherein the system for guiding formal verification of a circuit design to optimize time required for verification process further comprises Productivity Choice Determination tool to determine high-productivity choices for expanding the analysis region if verification fails.

Claim 32 would be allowable because the prior art does not teach or suggest the system for guiding formal verification, wherein the system for guiding formal verification of a circuit design to optimize the time required for verification process further comprises an articulation Point Selection tool to identify articulation points corresponding to the analysis region to choose smaller analysis region for circuit verification.

Claim 33 would be allowable because the prior art does not teach or suggest the system for guiding formal verification, wherein the system for guiding formal verification of a circuit design to optimize time required for verification process further comprises a Ruler Verifier for verifying user defined rules for the analysis region.

Claim 34 would be allowable because the prior art does not teach or suggest the system for guiding formal verification, wherein the system for guiding formal verification of a circuit design to optimize time require for verification process further comprises a database for storing a set of triples based on a set of signals selected by the user.

Claim 35 would be allowable because the prior art does not teach or suggest the system for guiding formal verification, wherein the GUI comprises a Source Code window for enabling the user to select a signal from a source code displayed.

Claim 36 would be allowable because the prior art does not teach or suggest the system for guiding formal verification, wherein the GUI comprises a Plot window for enabling the user to select a signal at a specific time cycle from the waveform of the signal displayed to the user.

Claim 37 would be allowable because the prior art does not teach or suggest the system for guiding formal verification comprising:

1. a Productivity Choice Determination tool to determine high-productivity choices for expanding the analysis region if verification fails;
2. an Articulation Point Selection tool to identify the articulation points corresponding to the analysis region to choose smaller analysis region for circuit verification,
3. a Rule Verifier for verifying user defined rule for the analysis region, and
4. a database for storing a set of triples based on a set of signals selected by the user. .

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1) Harding et al. (US Patent No. 6099575) disclose a method and apparatus for efficiently determine whether a set of constraints input to a verification tool are mutually contradictory or over constraining.

2) Tsuchiya (US patent No. 6449750) discloses a design verification device, a method, and memory medium for a semiconductor integrated circuit, capable of effectively introducing the formal verification in a higher-level design and capable of constructing a high-speed function verification environment with high verification assurance.

3) Martin et al. (US Patent Pub. No. 2003/0115562) disclose a design verification system and method for verifying an implementation design is functionally equivalent to a predetermined functionality of a reference design.

4) Alur et al. (US Patent No. 5483470) disclose an apparatus that employs a computationally tractable technique for developing and verifying systems.

5) R.E. Bryant ("Graph-Based Algorithms for Boolean Function Manipulation", IEEE Transactions on Computers, Vol. C-35, No. 8, August 1986) discloses a new data structure and a graph-based algorithms for manipulating Boolean function.

6) Dong Wang et al. (" Formal property Verification by Abstraction refinement with Formal, Simulation and Hybrid Engines", Carnegie Mellon Univ., DAC 2001) disclose a formal property verification tool based on abstraction refinement technique.

7) C. Kern et al. (" Formal Verification in Hardware Design: A survey", ACM Trans. on Design Automation of Electronic Systems, Vol. 4, No.2, April 1999, P.123-193) disclose a variety of formal methods and verification techniques in hardware design.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuyen To whose telephone number is (571) 272-8319. The examiner can normally be reached on 9:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuyen To
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